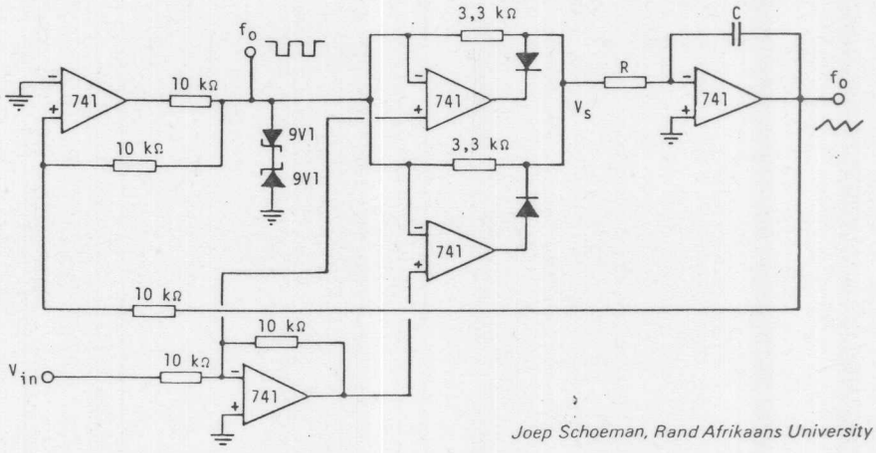
ngineer's notebook

Linear voltage-to-frequency converter outputs triangular and square waves

The circuit shows a linear voltage-to-frequency converter with both a triangular and squarewave output. The comparator and the integrator form a conventional simple function generator, generating the waveforms shown, while the clamps determine the amplitude of the squarewave applied to the integrator. The inverter provides the correct polarity of reference voltage to the negative clamp.

Component values have been selected so that $V_s \simeq V_{in}$ and $O < V_{in} < +10$. The proportionality between f_0 and V_{in} may be selected at any value, provided the operational amplifier slew rate and offsets are kept in mind. A suitable value is f_0 = 100 Hz/V while 1 000 Hz/V approaches the upper limit of a 741 with a 20 V p-p output. For f_0 = 100 Hz/V, CR ≃ 250 µs decreasing to 25 µs for 1 000 Hz/V.



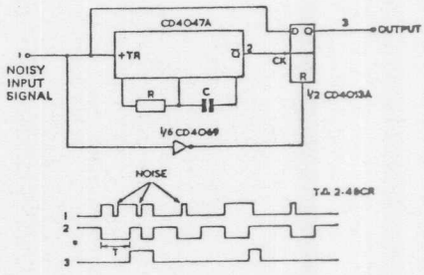
Joep Schoeman, Rand Afrikaans University

A noise discriminator for transducer outputs

The circuit diagram is of a simple noise discriminator using standard CD4000 Series COS/MOS integrated circuits. The circuit is designed so that all input pulses with a pulse width shorter than that defined by the monostable time will not appear at the output.

The output will have its negative-going edges coincident with the inputs, but will be reduced in pulse width by the monostable time.

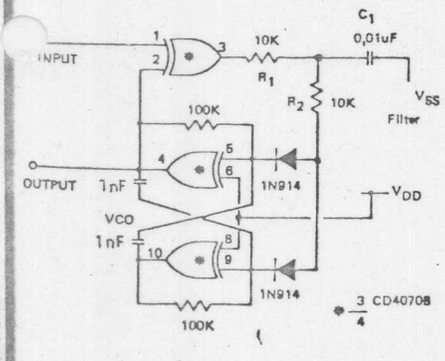
This circuit should be particularly useful in 'cleaning up' noise in transducer outputs where counting of pulses is involved. False counts due to noise spikes will be completely eliminated.



Information from Allied Electric

Phase-locked loop uses COS/MOS Exclusive OR gates

A complete phase-locked loop circuit, including a voltage-controlled oscillator, phase comparator and filter, can be made from three-quarters of a CD4070B exclusive OR gate COS/MOS integrated circuit. The circuit produces a square-wave output in quadrature with the input signal. The lock and capture ranges are determined by the values of the filter, R_1, R_2 and C_1.



For the circuit shown, the centre frequency is nominally 10 kHz. The loop can capture the input frequency over better than a 1,5:1 range and track over a 4:1 range. The loop will also lock to input signals that are multiples of the voltage-controlled oscillator frequency.

Information from Allied Electric.

Motor control using COS/MOS logic circuits

The CD40107B dual 2-input NAND buffer driver is a COS/MOS logic integrated circuit providing a high output sink current capability (typically 120 mA at a 10 V drive voltage) for relay, light-emitting-diode display, and other line-driver applications. Figures 1 and 2 show two simple motor control circuits incorporating this device.

Figure 1 illustrates how the addition of two p-n-p transistors to the dual NAND buffer gives a complementary output drive. This is used to drive the motor in the forward or reverse direction with a logic input. The application of a logic '0' at B stops the motor irrespective of the state of input A, and provides a degree of dynamic braking.

In the circuit of Figure 2, cross-coupling is used to give pulse logic control of the motor. Different logic states at the control inputs A and B result in the following motor functions: 0,0: off; 1,0: counter-clockwise; 1,1: as previous state; 0,1: clockwise; and 1,1 as previous state.

Information from Allied Electric.

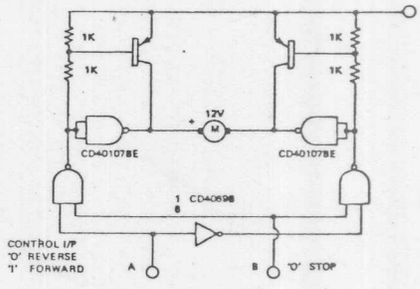


Figure 1.

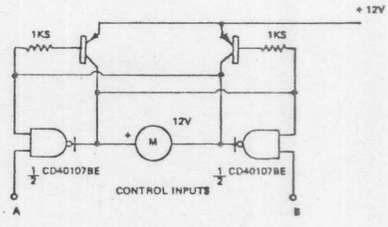


Figure 2.